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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,449	03/09/2000	Jun Hee Kim	40706.00009	2925

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EXAMINER

NGUYEN, CHANH DUY

ART UNIT PAPER NUMBER

2675

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/522,449

Applicant(s)

KIM ET AL.

Examiner

Chanh Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 6-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Remarks

1. The remarks filed on July 26, 2004 has been entered and considered by examiner.

Drawings

2. The drawings filed on March 09, 2000 have been approved.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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5. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al (U.S. Patent No. 6,121,947) in view of Kesatoshi (U.S. Patent No. 5,874,937) and Ueda et al (U.S. Patent No. 5,739,887) and further in view of Ninomiya et al (U.S. Patent No. 5,532,935).

As to claim 1, Furuhashi discloses a liquid crystal monitor drive apparatus for driving a liquid crystal panel including a connector for inputting an analog graphic signal (e.g., an analog video signal 102 from computer 101 inputted to A/D converter 104). It is well-known in the art to have clock signal inputted to the computer (for example, examiner cites the reference of Mitra et al U.S. 5,422,807 to show clock inputs 20 inputted to computer 10, even acknowledged by applicant on the related art Figure 2, page 4, lines 21-22 of the specification). Furuhashi teaches an analog-digital converter (104) arranged to convert the analog graphic signal (102) from the connector into digital graphic data, a scaler (118) for scaling the definition of the digital graphic data, a timing controller (120) arranged to drive the liquid crystal panel based on the digital graphic data from the scaler. Furuhashi does not teach a scaler for timing of the digital graphic data as recited in the claim. In fact, Furuhashi teaches the "timing" as recited in the claim outside the scaler (118) Kesatoshi teaches a scaler (36) for timing of the digital graphic by adjusting the timing of the graphic data based on the clock signal and adjusting the horizontal and vertical synchronous signals from the connector to match with a timing of the liquid crystal panel (see figure 3, column 4, lines 9-67 and column 6 line 61 through column 7, lines 12 and column 8, lines 14-26). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made

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to have used the scaler having timing adjusting to the scaler of Furuhashi so as to reduce the size of LCD driver.

The only thing different from the reference of Furuhashi and Kesatoshi and claim 1 is that Furuhashi and Kesatoshi do not mention an integrated circuit and a peripheral circuit coupled to inverter for driving a back light unit. It would have been obvious to one of ordinary in the art to have combine a number of electronic components into an integrated circuit so that the device is more compact. Ueda teaches integrated circuit driver (IC) and multi-layered flexible substrate display controller (101). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used an integrated circuit as taught by Ueda or Ito or prior art to the liquid crystal display device of Furuhashi as modified by Kesatoshi so as to reduce the display device size and weight; see column 7, lines 23-34 of Ueda.

Furuhashi, Kesatoshi and Ueda do not mention a peripheral circuit coupled to inverter for driving a back light unit. In same field of endeavor, Ninomiya teaches a peripheral circuit (43) coupled to an inverter (45) for driving back light unit (47); see figure 1. Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have added a peripheral circuit coupled to inverter for driving backlight as taught by Ninomiya to the liquid crystal device control device of Furuhashi as modified by Kesatoshi and Ueda so that the current supplied to the back light can be reduced in response to the lower analog signal, thereby reducing power consumption (see column 8, lines 53-58 of Ninomiya).

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As to dependent claims 2-5, these claims are met by Furuhashi combining with the device of Ueda or Ito or prior art. That is Furuhashi teaches the analog-digital converter (104), the scaler (118), and the timing controller (120) recited in claim 3 as well as the frame memory (110) connected with the scaler as recited in claims 2-4 and 5.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi in view of Kesatoshi, Ueda and Ninomiya et al as applied to claim 1 above, and further in view of Oshima et al (U.S. Patent No. 6,535,985).

As to claim 19, note the discussion of Furuhashi, Kesatoshi, Ueda and Ninomiya, none of them mentions the peripheral circuit operating with a frequency signal much lower than that of the clock signal. Oshima teaches a peripheral circuit (i.e. first processor 4) coupled to back light unit (25) operating with a frequency signal much lower than that of the clock signal (i.e. clock frequency of a second processor 7); see column 8, lines 8-12. Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have provided a peripheral circuit operating with a frequency signal much lower than that of the clock signal as taught by Oshima to the liquid crystal display control unit of Furuhashi as modified by Kesatoshi, Ueda and Ninomiya so that the service life of batteries will largely be increased.

Response to Arguments

7. Applicant's arguments filed July 26, 2004 have been fully considered but they are not persuasive.

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As to Drawings, the drawings have been approved as applicant's request.

As to Rejection under 35 U.S.C. §103(a), on page 10, first paragraph applicant argues that nowhere does Kesatoshi discuss a scaler which adjusts the horizontal and vertical synchronous signals to match with a timing of the liquid crystal panel. Examiner disagrees with applicant this point of view since Kesatoshi clearly teaches adjusting timing base clock signal (see column 4, lines 39-65) and adjusting the horizontal, vertical sync to match with a timing of the liquid crystal (column 4, lines 39-65). The timing of writing operation carried out by DCK1, HSYNC1 and VSYNC1 is adjusted so that it can be used as display synchronizing signals for the LCD panel (see column 4, lines 59-62). Claim 1 of Kesatoshi teaches that "scaling means for scaling the video image expressed by the video signal in the first format by utilizing the synchronizing signals and the determined image size so that the video signal is output in the second format of the second display device". Thus, the input signal including timing, sync signal must be changed so that it can be match to display format. If these input timing and sync signals is not match to the display device, then it is impossible to display the image on the screen or the image can be displayed with the distortion. That is not what Kesatoshi is desired.

Applicant acknowledges that "Kesatoshi is directed to adjusting the resolution of the input video signal to be coincident with the resolution of the display device based on the dot clock signal DCK1, sync signal HSYNC1 and VSYNC1" (see Remarks page 10, lines 4-7). Thus if the resolution of the input video signal is different from the display, then the timing as well as the sync signal of the video must be changed (see Figure 4).

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For example, the resolution of the input video signal is 640 x 400, but the display device has resolution 640 x 480, then horizontal frequency sync signal changes from 24.8 to 37.5 and vertical sync signal also changes from 56.4 to 72 (see Figure 4).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chanh Nguyen whose telephone number is (703) 308-6603.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231


or faxed to:

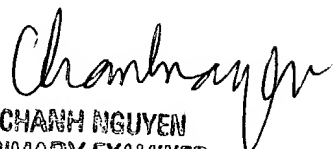
(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121

Crystal Drive, Arlington, VA, Sixth Floor (Receptionist)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.


C. Nguyen
October 30, 2004


CHANH NGUYEN
PRIMARY EXAMINER